What is claimed is:

1. A CMOS image sensor, comprising:

an image capturing means for converting light incident upon a photo-sensitive area to an analog image signal;

an analog-to-digital converter for converting the analog image signal to a digital image signal; and

a ramp signal generator for producing a ramp signal in order to provide a reference voltage signal to the analog-to-digital converter, the ramp signal generator including:

a plurality of capacitors and switches;

an amplifier coupled to the plurality of capacitors and switches for receiving gain and reset voltages from external circuitry; and

capacitance controlling means coupled in parallel to at least one of the plurality of capacitors in the ramp signal generator in order to form the ramp signal for an analog gamma correction.

2. The CMOS image sensor as recited in claim 1, wherein the plurality of switches in the ramp signal generator are selectively operated in response to control signals from a digital controller in the CMOS image sensor.

3. The CMOS image sensor as recited in claim 2, wherein the capacitance controlling means includes the plurality of capacitors and the plurality of switches to

selectively connect the plurality of capacitors to the amplifier in response to the control signals from the digital controller.

4. The CMOS image sensor as recited in claim 2, further comprising:

counting means for creating a digital counting value based on a result signal from a chopper comparator; and

a latch circuit for storing the digital counting value from the counting means.

5. A CMOS image sensor, comprising:

an image capturing means for capturing an analog image signal from an object;

an analog-to-digital converter to convert the analog image signal to a digital image signal; and

a ramp signal generator producing a ramp signal in order to provide a reference voltage signal to the analog-to-digital converter, said ramp signal generator including:

a first switch connected to a gain voltage;

a plurality of second switches connected in parallel to the first switch;

a plurality of capacitors connected to the second switches;

a third switch connected between the first switch and a ground voltage level;

a fourth switch commonly connected to the plurality of capacitors and connected to a reset voltage;

a fifth switch connected to the plurality of capacitors;

an amplifying means for receiving the reset voltage and receiving the gain voltage via the fifth switch for outputting the ramp signal;

a sixth switch connected in parallel to the amplifying means; and

a capacitor connected in parallel to the sixth switch.

6. The CMOS sensor as recited in claim 5, wherein the plurality of capacitors and the second switches in the ramp signal generator are selectively connected to each other in response to control signals from a digital controller in the CMOS image sensor.